REMARKS

I. INTRODUCTION

Claims 1-24, 26-28, and 32 have been amended and remain pending in the present application. No new matter has been added. In view of the above amendments and following remarks, it is respectfully submitted that all of the presently pending claims are allowable.

II. THE 35 U.S.C. § 103(a) REJECTIONS SHOULD BE WITHDRAWN

The Examiner has rejected claims 1-24, 26-28, and 32 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent Application No. 202/0016880 to Bhagat (hereinafter "Bhagat") in view of "ARM® Application Note 25: Exception Handling on the ARM® (Including THUMB-aware Processors)" (hereinafter "Note 25") in further view of "ARM® Application Note 31: Using EmbeddedICE" (hereinafter "Note 31").

Bhagat discloses an interrupt controller 106 for more economical THUMB program execution by using an interrupt service routine (ISR) preamble coded in ARM® program code. (*Bhagat*, Abstract). An ARM® processor 102 is capable of running two instruction sets ARM 32-bit instructions and THUMB 16-bit instructions. Although the ARM 32-bit instructions offer higher performance, they utilize more code space than the THUMB 16-bit instructions. (*Id.*, paragraph 0007). When an interrupt request is received, the processor 102 switches to ARM execution mode. Bhagat discloses an interrupt controller with an execution and disable control bit to facilitate the switching between the ARM and THUMB modes during interrupt request processing to minimize code space usage. (*Id.*, paragraph 0035).

Notes 25 and 31 disclose a method for utilizing ARM architecture to handle IRQ and FIQ interrupts, giving the higher priority FIQ interrupt ability to interrupt regular priority IRQ exception calls.

In contrast, claim 1 of the present application recites a method for sequentially executing interrupt requests regardless of their priority by "merging a first type interrupt and a second type interrupt into a single service routine upon receipt of the first type interrupt and the second type interrupt by a processor having an interrupt vector table for *operationally sequential placement and execution of a first type vector address corresponding to the first type interrupt and a second type vector address corresponding to the second type interrupt, the second type interrupt having a higher priority than the first type interrupt.*"

The present invention is directed to preventing higher priority FIQ interrupt requests from taking precedence over regular priority IRQ interrupt requests. Once an interrupt request is received it is processed regardless of the priority of *subsequent* interrupt requests. For instance, even if the current request is an IRQ request and the subsequent request is a higher priority FIQ request, the subsequent FIQ request will not interfere in the execution of the original request. Thus, the interrupt requests are processed based on their sequential listing in the vector table and not the priority.

Conversely, Bhagat does not teach or suggest "operationally sequential placement and execution of a first type vector address corresponding to the first type interrupt and a second type vector address corresponding to the second type interrupt, the second type interrupt having a higher priority than the first type interrupt" as recited in independent claim 1 of the present application. In Bhagat:

> Interrupt vectoring preferably uses a fixed-priority interrupt vector table. A vector priority is provided for each of the FIQ and IRQ interrupts 128 and 130. The FIQ interrupt 128 always has a higher priority than the IRQ interrupt 130 in ARM7TDMI processor 102.

Bhagat, paragraph 0030.

Bhagat not only fails to disclose using a vector table that lists the interrupt vectors sequentially regardless of the priorities of the interrupt requests, it specifically requires that the vectors have the same priority as the interrupt requests to which they are linked. Bhagat's invention is only concerned with switching between ARM and THUMB modes during interrupt request processing. The conventional practice of processing higher priority requests, such as FIQ interrupt requests is unchanged as illustrated in Bhagat's disclosure which specifically provides for interruption of processing of lower priority interrupt requests when the ISR preamble is disabled:

> Because a higher-priority interrupt may occur between the execution of the ISR preamble and the execution of the corresponding ISR program code, the contents of ISRINST register 314 are preserved from the time the IRQINST register is read to the time the ISRINST register 314 is read. The ISRINST register is updated immediately thereafter.

Bhagat, paragraph 0039.

Neither Bhagat, Note 25 or Note 31, either alone or in combination, include any showing or suggestion of sequentially executing interrupt requests regardless of their priority by "merging a first type interrupt and a second type interrupt into a single service routine upon receipt of the first type interrupt and the second type interrupt by a processor having an interrupt vector table for *operationally sequential placement and execution of a first type vector address corresponding to the first type interrupt and a second type vector address corresponding to the*

second type interrupt, the second type interrupt having a higher priority than the first type interrupt" as recited in independent claims 1, 19 and 24 of the present application. It is therefore respectfully submitted that claims 1, 19 and 24 are allowable. Because claims 2-8 and 20-23 depend from and, therefore, include all of the limitations of claims 1 and 19 respectively, it is respectfully submitted that these claims are also allowable and the rejection of claims 1-8 and 19-24 under 35 U.S.C. § 103(a) should be withdrawn.

Independent claim 9 includes the same limitation as claim 1, i.e., "*merging IRQ interrupts and FIQ interrupts into a single service routine upon receipt of the IRQ and FIQ interrupts by a processor having an interrupt vector table for operationally sequential placement and execution of IRQ vector addresses corresponding to the IRQ interrupts and an FIQ vector addresses corresponding to the FIQ interrupts.*" Thus, for the reasons described above with reference to claim 1, it is respectfully submitted that claim 9 is also allowable. Because claims 10-14 depend from and, therefore, include all of the limitations of claim 9, it is respectfully submitted that these claims are also allowable and the rejection of claims 9-14 under 35 U.S.C. § 103(a) should be withdrawn.

Independent claims 15 and 17 include the same limitation as claim 1, i.e., "*receiving first type interrupts and second type interrupts, at operationally sequentially placed first type and second type interrupt vector addresses, the first type vector address corresponding to the first type interrupts and the second type vector address corresponding to the second type interrupts, the second type interrupts having a higher priority than the first type interrupts.*" Thus, for the reasons described above with reference to claim 1, it is respectfully submitted that claims 15 and 17 are allowable. Because claims 16 and 18 depend from and, therefore, include

all of the limitations of claims 15 and 17 respectively, it is respectfully submitted that these claims are also allowable and the rejection of claims 15-18 under 35 U.S.C. § 103(a) should be withdrawn.

Independent claim 26 includes the same limitation as claim 1, i.e., "a first interrupt mode and a second interrupt mode to respectively accept interrupt requests of first and second types, the second interrupt mode having a higher priority that the first interrupt mode, both first and second interrupt modes being disableable to selectively reject interrupt requests of the first and second interrupt types" and "a first vector address operatively associated with receipt of interrupt requests of the first type, and a second vector address operatively associated with receipt of interrupt requests of the second type, the first vector address operationally preceding the second vector address in the vector table." Thus, for the reasons described above with reference to claim 1, it is respectfully submitted that claim 26 is allowable. Because claims 27 and 28 depend from and, therefore, include all of the limitations of claim 26, it is respectfully submitted that these claims are also allowable and the rejection of claims 26-28 under 35 U.S.C. § 103(a) should be withdrawn.

Independent claim 32 includes the same limitation as claim 1, i.e., "providing a processor having a first interrupt mode for accepting interrupt requests of a first type at a first type vector address, and a second interrupt mode for accepting interrupt requests of a second type at a second type vector address, the second interrupt mode having a higher priority than the first interrupt mode, both first and second interrupt modes being selectively disableable to selectively reject interrupt requests of the first and second interrupt requests of the first and second interrupt types." Thus, for the reasons described above with reference to claim 1, it is respectfully

submitted that claim 32 is not unpatentable over Bhagat in view of Note 25 in further view of Note 31 and the rejection of claim 32 under 35 U.S.C. § 103(a) should be withdrawn.

CONCLUSION

In light of the foregoing, the applicants respectfully submit that all of the now pending claims are in condition for allowance. All issues raised by the Examiner having been addressed, an early and favorable action on the merits is earnestly solicited.

Respectfully submitted,

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